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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,694	02/28/2002	Gary J. Kovar	SC11763TK	1627

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EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,694	KOVAR ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-16,18-21 and 32-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-16,18-21 and 33-36* is/are allowed.

6)☒ Claim(s) *1,2,6-12,32 and 37-42* is/are rejected.

7)☒ Claim(s) *3 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgment

1. The amendment filed on 12/10/2003 in response to the Office action mailed on 09/05/2003 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-4, 6-16, 18-21 and 32-42.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 6-12, 32 and 37-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Iketani (US 20020016013, cited by Applicant).

4. Regarding claim 1, Iketani (e.g. figs. 1-10) shows a method for testing a plurality of semiconductor dies, wherein the method comprises the steps of:

- Providing a semiconductor wafer (pp 0002);
- Singulating the semiconductor wafer to form a plurality of semiconductor die 33 (e.g. fig. 3 & pp 0002);

- Encapsulating the plurality of semiconductor die to form an array 20 (e.g. fig. 5A);
- Placing the array on a temporary substrate 50 on a testing platform 51 (e.g. fig. 6A/B);
- Testing at least one of the plurality of semiconductor dies in the array while the array is on the temporary substrate and the testing platform (e.g. fig. 8A/B);
- Removing the temporary substrate and sorting the array; (e.g. fig. 10A).

5. Regarding claim 2, Iketani shows that the temporary substrate is a temporary adhesive substrate (pp 0052)

6. Regarding claim 6, Iketani shows that the method further include attaching the plurality of semiconductor dies to a package substrate 21 and electrically connecting at least one of the plurality of semiconductor dies to the package substrate (e.g. fig. 12A).

7. Regarding claim 7, Iketani shows that the method includes the step of electrically isolating the plurality of semiconductor dies (e.g. fig. 10A).

8. Regarding claim 8, Iketani shows that the electrically isolation is performed by using a saw 36 (e.g. fig. 7A).

9. Regarding 9, Iketani shows that method further comprises the step of singulating the plurality of semiconductor die in the array to physically separate at least two-semiconductor die of the plurality of semiconductor die from each other (e.g. fig. 7A).

10. Regarding claim 10, Iketani shows that the singulating is performed by sawing (e.g. fig. 7A).

11. Regarding claim 11, Iketani shows that the step of encapsulating of the plurality of semiconductor die can be accomplished by molding (pp 0002).

12. Regarding claim 12, Iketani shows that the method includes testing in parallel at least two of the plurality of the semiconductor dies (e.g. fig. 9A).

13. Regarding claim 32, Iketani shows that the electrical isolating is performed using a partial saw process prior to testing. After testing the plurality of semiconductor die are diced to physically separate at least two-semiconductor die of the plurality of semiconductor die from each other (e.g. figs. 7 & 8).

14. Regarding claim 37, Iketani (e.g. figs. 1-10) shows a method for testing a plurality of semiconductor dies, wherein the method comprises:

- Providing a plurality of semiconductor die 33 (e.g. fig. 3 & pp 0002);
- Encapsulating the plurality of semiconductor die 33 to form an array 20 (e.g. fig. 5A);
- Placing the array on a temporary substrate 50;
- Electrically isolating the plurality of semiconductor die in the array using a partial saw process (e.g. fig. 7A);
- Placing the array with the temporary substrate on a testing platform 51 (e.g. fig. 6A/B);

- Testing at least one of the plurality of semiconductor dies in the array while the array is on the temporary substrate and the testing platform (e.g. fig. 8A/B);
- And removing the temporary substrate (e.g. fig. 10A).

15. Regarding claim 38, Iketani shows that the step of attaching the plurality of semiconductor die 33 to a package substrate 21; and electrically connecting at least one of the plurality of semiconductor die to the package substrate (e.g. fig. 4).

16. Regarding claim 39, Iketani shows that the electrically isolation is performed by using a saw 36 (e.g. fig. 7A).

17. Regarding claim 40, Iketani shows that after the testing, a fully singulating of the dies in the array is performed to physically separate at least two dies from each other (e.g. figs. 7-10A).

18. Regarding claim 41, Iketani shows that the singulating is performed by sawing (e.g. fig. 7A).

19. Regarding claim 42, Iketani shows that the temporary substrate is a temporary adhesive substrate (pp 0052).

Allowable Subject Matter

20. Claims 13-16, 18-21 and 33-36 are allowed.

21. Claims 3 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

22. Applicant's arguments with respect to claims 1 and 37 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

23. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 12/18/2003 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

25. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

26. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leonardo Andújar
Patent Examiner Art Unit 2826
LA
3/19/04

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